REMARKS

Claims 1-3, 5-9, and 12-16 remain in the application. Claims 4, 10, and 11 have been canceled. Claims 1, 7, 9, and 12 have been amended.

In the first Office Action mailed March 29, 2005, the Examiner rejected claims 1-16 under 35 U.S.C. § 103(a) as unpatentable over applicant's Background description of Figures 1 and 2 in view of U.S. Patent No. 6,127,723 ("Aiello et al.").

Applicant respectfully disagrees with the basis for the rejection and requests reconsideration and further examination of the claims.

The disclosed embodiment of the invention will now be discussed in comparison to the applied reference. Of course, the discussion of the disclosed embodiment and the discussion of the differences between the disclosed embodiment and the subject matter described in the applied reference do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely assist the Examiner in appreciating important claim distinctions discussed thereafter.

In the embodiment of the invention to which the claims are directed, a Zener element is connected between the base of a high voltage bipolar transistor and a common terminal of the emitter of the high voltage transistor and a drain of a low voltage MOS transistor. Advantageously, the Zener diode limits the base-emitter junction voltage value of the high voltage bipolar transistor, whose breakdown value is quite lower than the low voltage MOS transistor. Thus, the Zener diode serves as a clamp to the voltage increase at the drain terminal of the MOS transistor, which is not in a breakdown condition. This is because the Zener voltage of the diode is lower than the breakdown voltage of the bipolar transistor base-emitter junction. With the configuration of the present invention, a low voltage MOS transistor with a low breakdown voltage and, subsequently, a low conduction resistance Ron, can be used, which increases the current capacity of the entire monolithic structure implementing such emitter-switching configuration.

In order for this configuration to function, the diode must be connected such that the anode is coupled to the base or control terminal of the bipolar transistor and the cathode is coupled to the common conduction terminal of the emitter of the high voltage bipolar transistor and the drain of the low voltage MOS transistor.

In contrast, Aiello et al., U.S. Patent No. 6,127,723, describe an integrated device in an emitter-switching configuration in which a Zener diode has its cathode terminal coupled to the base of a first transistor and its anode coupled to the emitter of a second transistor that is series coupled to the first transistor. This configuration is designed to speed up the turn off process of the power actuator (quenching process), which is the first transistor. This reverse polarity connection taught by Aiello et al. does not increase the current capacity of the integrated circuit. Rather, Aiello et al. expressed objective is to reduce the quenching time of the device and thus reduce power dissipation thereof. This clearly has nothing to do with increasing the robustness of the power actuator, which is one purpose of the present invention.

Turning to the claims, claim 1 is directed to an emitter switching configuration that comprises at least one bipolar transistor and a MOS transistor having a common conduction terminal, and a Zener diode inserted between a common control terminal of the bipolar transistor and the common conduction terminal, the Zener diode having an anode terminal coupled to the control terminal of the bipolar transistor and a cathode terminal connected to the common conduction terminal of the bipolar transistor. As discussed above, nowhere do Aiello et al. teach or suggest modifying the circuit in Figure 1 of the present invention with a Zener diode having an anode terminal coupled to the control terminal of the bipolar transistor and a cathode terminal connected to the common conduction terminal of the bipolar transistor. Rather, if one were to combine the description of Aiello et al. with the known emitter switching configuration shown in Figure 1 of the present application, the result would be a Zener diode having an anode coupled to the base of the bipolar transistor and a cathode coupled to the source of the MOS transistor. Such a coupling of the Zener diode would fail to achieve the combination of claim 1 or to function in accordance with its purposes.

In view of the foregoing, applicant respectfully submits that claim 1 is clearly allowable over the combination cited by the Examiner because such is not taught or suggested by the combination made by the Examiner.

Dependent claims 2-6 are allowable for the reasons why claim 1 is allowable in addition to the features recited therein. Moreover, in claim 2, the Zener diode is recited as having a lower Zener voltage than a breakdown voltage of a junction between the control terminal of the bipolar transistor and the conduction terminal of the bipolar transistor. Clearly,

there is no teaching or suggestion in Aiello et al. for such a breakdown voltage configuration of the Zener voltage and the bipolar transistor.

Claim 7 is directed to a monolithic structure effective to implement an emitter switching configuration that has at least one bipolar transistor and a MOS transistor having a common conduction terminal, and wherein a Zener diode is defined in the structure to be in parallel with a junction defined by first and second buried layers such that an anode of the Zener diode is coupled to the control terminal of the bipolar transistor and a cathode is coupled to the common conduction terminal of the bipolar transistor. Applicant respectfully submits that claim 7 is allowable for the reasons discussed above with respect to claim 1, *i.e.*, nowhere does the combination of Aiello et al. and Figure 1 of the Background description of the present invention teach or suggest such a Zener diode - bipolar transistor configuration. Claim 8, which depends from claim 7, is also allowable for the reasons why claim 7 is allowable in addition to the features recited therein.

Claim 9 is directed to an emitter switching circuit that comprises a bipolar transistor having a base-to-emitter device coupled to a drain terminal of a MOS transistor and configured to prevent a breakdown condition of a body-drain junction of the MOS transistor, the base-to-emitter device comprising a Zener diode configured to have a breakdown voltage that is less than a breakdown voltage of the base emitter junction of the bipolar transistor. The Aiello et al. reference when combined with Figure 1 of the present application clearly would not achieve the combination recited in claim 9, *i.e.*, the Zener diode configured to have a breakdown voltage less than the breakdown voltage of the base-emitter junction of the bipolar transistor. This is because Aiello et al. teaches a reverse polarity coupling of the diode between the base of the bipolar transistor and a source of a low voltage MOS transistor. One of ordinary skill would not be motivated to combine these two references in the manner the Examiner suggests because it would fail to achieve the functionality of the claimed circuit. Applicant respectfully submits that claim 9 is allowable over the combination of Aiello et al. and Figure 1 of the present application. Claim 12, which depends from claim 9, is also allowable for the reasons why claim 9 is allowable as well for the additional features recited therein, *i.e.*, the diode having an anode terminal connected to a base terminal of the bipolar transistor and a cathode terminal connected to an emitter terminal of the bipolar transistor, for the reasons discussed above.

Independent claim 13 is directed to an integrated emitter switching circuit that comprises a substrate of first conductivity having first and second layers formed thereon and an epitaxial layer covering these layers, and first and second wells formed in the epitaxial layer to define a Zener diode having an anode terminal connected to a base terminal of a bipolar transistor and a cathode terminal coupled to an emitter terminal of the bipolar transistor that is also coupled to a drain terminal of a MOS transistor formed in association with an epitaxial layer. Applicant respectfully submits that claim 13 is clearly allowable over the combination recited by the Examiner of Aiello et al. and Figure 1 of the present invention because nowhere does this combination teach or suggest the Zener diode having an anode terminal connected to base terminal of the bipolar transistor and a cathode terminal coupled to an emitter terminal of the bipolar transistor and a drain terminal of a MOS transistor as discussed above. Applicant respectfully submits claim 13 and dependent claims 14-16 are clearly allowable.

In view of the foregoing, applicant submits that all of the claims remaining in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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